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TITLE: PACKAGE STRUCTURE

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INVENTOR-INFORMATION:

NAME

TOYODA, AKIKAZU

NOSE, TSUNETARO

YADOKORO, HIROAKI

KOYATA, SAKAE

ASSIGNEE-INFORMATION:

NAME

COUNTRY

MITSUBISHI MATERIALS CORP

N/A

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US-CL-CURRENT: 257/664

ABSTRACT:

PURPOSE: To enable a package structure to be of surface mounting type and to be easily matched to an external circuit in impedance by a method wherein a transmission line such as a micro-strip line is formed throughout a surface-side signal line and a rear-side signal line and controlled in specific impedance by through-holes.

CONSTITUTION: An insulating board 44 provided with through-holes 56 and 58 where a semiconductor chip 42 is mounted, a rear-side ground pattern 52 formed on the rear of the insulating board 44, and a front-side ground pattern 48 connected to the rear-side ground pattern 52 are provided. A surface-side

signal line 46 which forms a transmission line with the surface-side ground pattern 48 and/or the rear-side ground pattern 52 and a rear-side signal line 50 which forms a micro-strip line with the surface-side ground pattern 48 connected to the surface-side signal line 46 are provided. By this setup, a package structure of this design can be easily matched to an outer circuit in impedance.

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(71)出願人 000006264

三菱マテリアル株式会社

東京都千代田区大手町1丁目5番1号

(72)発明者 豊田 明和

埼玉県秩父郡横瀬町大字横瀬2270番地 三

菱マテリアル株式会社セラミックス研究所

内

(72)発明者 能勢 恒太郎

埼玉県秩父郡横瀬町大字横瀬2270番地 三

菱マテリアル株式会社セラミックス研究所

内

(74)代理人 弁理士 小杉 佳男 (外1名)

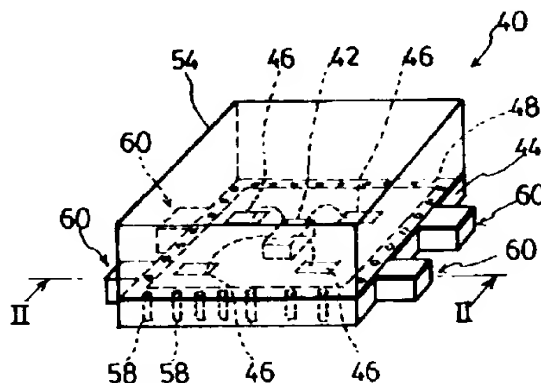
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(54)【発明の名称】 パッケージ構造体

(57)【要約】

【目的】 外部回路とのインピーダンス整合が容易で、表面実装できるパッケージ構造体を提供する。

【構成】 パッケージ構造体40は、表面に半導体チップ42が載置された絶縁基板44と、絶縁基板44の裏面に形成された裏面側グランドパターン52と、絶縁基板44の表面の周縁部を含む領域に形成され第2のスルーホール内の導体を介して表面側グランドパターン52と接続された表面側グランドパターン48と、絶縁基板44の表面に形成され半導体チップ42の入力端子又は出力端子と接続された、表面側グランドパターン及び/又は裏面側グランドパターンとの間で伝送線路を形成する表面側信号ライン46と、絶縁基板44の裏面に形成され第1のスルーホール内の導体を介して表面側信号ラインと接続された、表面側グランドパターン48との間でマイクロストリップラインを形成する裏面側信号ライン50と、絶縁基板44上の半導体チップ42と表面側信号ライン46とを被覆し表面側グランドパターン52と接続された導電性キャップ54とを備えた。



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【0009】

【実施例】以下、本発明の実施例を示す添付図面を参照しながら、本発明の実施例を説明する。図1は本発明の一実施例に係るパッケージ構造体40の斜視図、図2は図1のII-II断面図である。

【0010】このパッケージ構造体40は、半導体チップ12が載置された絶縁基板14と、この絶縁基板14の表面に形成された表面側信号ライン46と、絶縁基板14の表面に表面側信号ライン46を取り巻くように形成された表面側グランドパターン48と、絶縁基板14の裏面に形成され表面側信号ライン46と接続された裏面側信号ライン50（図2参照）と、絶縁基板14の裏面に形成され表面側グランドパターン48と接続された裏面側グランドパターン52（図2参照）と、絶縁基板14上の半導体チップ12と表面側信号ライン46とを被冠し表面側グランドパターン48と接続された導電性キャップ54とを備えている。

【0011】絶縁基板14は、信号ライン用の複数の第1のスルーホール56（図2参照）とグランド用の複数の第2のスルーホール58（図1参照）とを有する。また、表面側信号ライン46は半導体チップ12の入力端子又は出力端子と接続されており、この表面側信号ライン46は、裏面側グランドパターン52との間でマイクロストリップラインを形成している。また、裏面側信号ライン50は第1のスルーホール56内の導体を介して表面側信号ライン46と接続されており、表面側グランドパターン48との間でマイクロストリップラインを形成している。このマイクロストリップラインは、図1及び図2に示すように、本実施例では突出部60に形成されているため、表面実装時の位置が容易にわかりしたが、半留まりを向上させることができる。また、裏面側グランドパターン52は第2のスルーホール58内の導体を介して表面側グランドパターン48と接続されている。

【0012】次に、本実施例のパッケージ構造体40の製造方法について説明する。まず、アルミ基板などの絶縁基板14の外形とスルーホール56、58がクロウガスレーザにより加工される。次に、表面側信号ライン46のメタライズがAuの厚膜導体で形成され、表面側グランドパターン48、裏面側信号ライン50、裏面側グランドパターン52、およびスルーホールがAg-Pbの厚膜導体で形成される。次に、モノリシックマイクロウェーブ集積回路などの半導体チップ12がAu-Sn等の共晶ハンダで絶縁基板14上にダイボンディングされ、25μmのAuワイヤでボンディング配線される。次に、導電性キャップ54が表面側グランドパターン48上にパラレルシーム溶接法で溶接され、パッケージ構造体40が完成する。その後、絶縁基板14の裏面側が、この絶縁基板14の裏面のパターンと合致したパターンが形成されたマザーボードに、Sn-Pb等の共晶

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ハンダによりはんだ付けされる。

【0013】尚、本実施例のパッケージ構造体40の突出部60の形状は、図3に示すような突出部62の形状としてもよい。絶縁基板14の変形例を、図4に示す。図4からわかるように2枚の絶縁基板64、66を重ねて基板とすることもできる。この場合は、夫々の絶縁基板64、66にスルーホールが形成されて表面と裏面との信号ラインが接続される。

【0014】次に、キャップの材料をセラミックとした例を図5に示す。このセラミック製のキャップ70はその内壁72または外壁74がメタライズされており（図5では外壁がメタライズされている）、このメタライズされた面が絶縁基板14の表面のグランドパターンと接続されることによって、電磁遮蔽効果が得られる。キャップ70のメタライズは、スッキ、導電塗料の塗布、厚膜ペーストの塗布などにより行われる。

【0015】尚、上記実施例のパッケージ構造体では表面側信号ライン46は、裏面側グランドパターン52との間でマイクロストリップラインが形成されているが、表面側グランドパターンとの間でアプレーナ型ストリップライン、表面側及び裏面側グランドパターンとの間でグラウンドッドコプレーナ型ストリップラインを形成してもよい。

【0016】また、表面側信号ラインと裏面側信号ラインとの間にはスルーホール内の導体を介して接続されているため、このスルーホールの寸法等を調整することによって特性インピーダンスを例えば50Ωに合わせることができる。また、表面側グランドパターンと裏面側グランドパターンとの間にもスルーホール内の導体を介して接続されているため、このスルーホールの数を増やすことによって表面側のグランドを強化することができる。

【0017】

【発明の効果】以上説明したように、本発明のパッケージ構造体は、表面側信号ラインと裏面側信号ラインに亘ってマイクロストリップライン等の伝送線路が形成されしかもスルーホールによりその特性インピーダンスを調整することができる。したがって外部回路のインピーダンスを所定のインピーダンスに調整することにより容易に外部回路との間でインピーダンスが整合される。

【0018】また、このパッケージ構造体を回路基板に載置して裏面側信号ラインと回路基板上の配線パターンをハンダ等で接続することができ容易に表面実装が可能となる。

【1面の簡単な説明】

【図1】パッケージ構造体を示す斜視図である。

【図2】図1のII-II断面図である。

【図3】突出部の変形例を示す斜視図である。

【図4】絶縁基板を2枚重ねにした場合を示す断面図である。

【図5】セラミック製のキャップを使用した場合を示す

断面図である。

【図6】キャップで被冠される前の、従来のパッケージ構造体を示した図である。

【図7】図6に示す基板にキャップが被冠された場合を示す断面図である。

【図8】従来の他のパッケージ構造体を示す斜視図である。

【符号の説明】

40 パッケージ構造体

42 半導体チップ

44 絶縁基板

46 表面側信号ライン

48 表面側グランドパターン

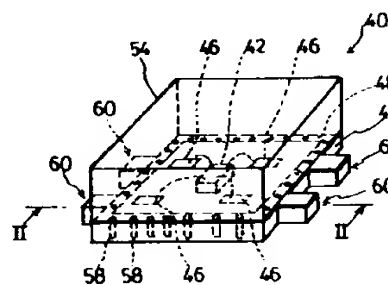
50 裏面側信号ライン

52 裏面側グランドパターン

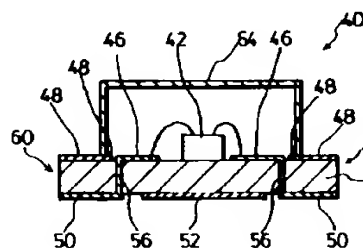
54 導電性キャップ

56、58 スルーホール

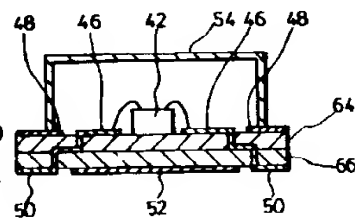
【図1】



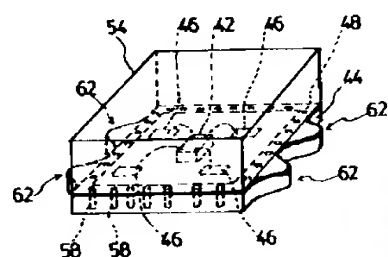
【図2】



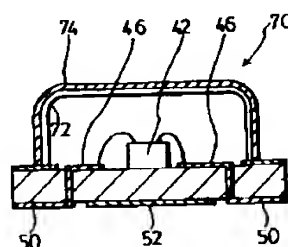
【図4】



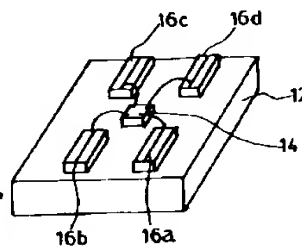
【図3】



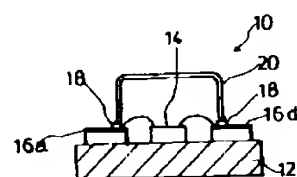
【図5】



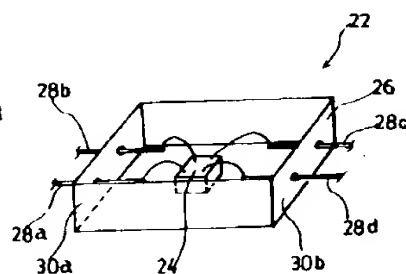
【図6】



【図7】



【図8】



フロントページの続き

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(72)発明者 谷所 博明
埼玉県秩父郡横瀬町大字横瀬2270番地 三
菱マテリアル株式会社セラミックス研究所
内

(72)発明者 古屋田 栄
埼玉県秩父郡横瀬町大字横瀬2270番地 三
菱マテリアル株式会社セラミックス研究所
内

To:
Attorney Mr. John Dresch (Reg. Nr.: 46,672)
SUGHRUE MION, PLLC
Fax Nr.: 202-293-7860

Topic : 09/664,094 (Docket No.: Q60884) / Certified Translation of Japanese Document
No. 5-166965.

Date: February 10, 2003

Dear Mr. Dresch:

With reference to our recent interview and interview summary on application 09/664,094,
please find the title page and 11 pages comprising the entire certified translation of
Japanese Doc. 5-166965.

Sincerely,



Johannes P. Mondt, Patent Examiner for 09/664,094 (Docket No.: Q60884) at Art Unit
2826.
(Tel. No.: (703-)306-0531)

PTO 2003-1432

Japan, Kokai

Document No. 5-166965

PACKAGE STRUCTURE

[Pakkegi Kozotai]

Meiwa Toyota, Tsunetaro Nose, Hiroaki Tanisho,
and Sakae Furuyada

UNITED STATES PATENT AND TRADEMARK OFFICE

Washington, D.C.

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Inventors : Meiwa Toyota, Tsunetaro Nose,
Hiroaki Tanisho, and Sakae Furuyada

Applicant : Mitsubishi Materials Corporation

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H 01 P 3/08

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English Title : PACKAGE STRUCTURE

Specification

/2

1. Title of the Invention: PACKAGE STRUCTURE

2. Claim

1. A package structure, characterized by the fact that being equipped with a semiconductor chip, an insulating substrate in which said semiconductor chip is placed on the surface and which has first through holes for a signal line and second through holes for a ground, a back face-side ground pattern formed on the back face of the above-mentioned insulating substrate, a surface-side ground pattern which is formed in a region including the peripheral edge part of the surface of the above-mentioned insulating substrate and connected to the above-mentioned back face-side ground pattern via a conductor in the above-mentioned second through holes, a surface-side signal line which is formed on the surface of the above-mentioned insulating substrate, connected to an input terminal or output terminal of the above-mentioned semiconductor chip, and forms a transmission line with the above-mentioned surface-side ground pattern and/or the above-mentioned back face-side ground pattern, a back face-side signal line which is formed on the back face of the above-mentioned insulating substrate, connected to the above-mentioned surface-side signal line via a conductor in the above-mentioned

¹ Numbers in the margin indicate pagination in the foreign text.

first through holes, and forms a microstrip line with the above-mentioned surface-side ground pattern, and an electroconductive cap which covers the above-mentioned semiconductor chip on the above-mentioned insulating substrate and the above-mentioned surface-side signal line and is connected to the above-mentioned surface-side ground pattern.

3. Detailed explanation of the invention

[0001]

(Industrial application field)

The present invention pertains to a package structure. In particular, the present invention pertains to a package structure suitable for packaging semiconductor chips of microwaves, monolithic integrated circuits, hybrid integrated circuits, etc.

[0002]

(Prior art)

The purpose of a package structure as a container of semiconductor elements is to draw out electric terminals and to prevent the faults and degradation of semiconductor chips by blocking the semiconductor chips from an external air. As such a package structure, for example, there are conventional package structures shown in Figures 6-8.

[0003] In a package structure 10 shown in Figures 6 and 7, a semiconductor chip 14 placed on a metal 12 and part of four lead terminals 16a, 16b, 16c, and 16d connected to input and output terminals of the semiconductor chip 14 are covered with a metal

cap 20 (not shown in Figure 6) via an electric insulator 18 such as ceramic and glass. Also, as shown in Figure 7, only the lead terminals 16a, 16b, 16c, and 16d are protruded as a microstrip line to the outside of the metal cap 20.

[0004] Also, in a package structure 22 shown in Figure 8, a semiconductor chip 24 is arranged in a box 26, and leads 28a, 28b, 28c, and 28d connected to input and output terminals of a semiconductor chip 24 are drawn out to the outside through walls 30a and 30b of the box 26.

[0005]

(Problems to be solved by the invention)

Various kinds of said package structures have been used. However, in the package structure 10 shown in Figure 7 among them, it is necessary to fix the entire part of the package structure 10 to a circuit substrate on which the package structure 10 is arranged by screws, and the surface mounting is impossible.

[0006] In the package structure 22 shown in Figure 8, since it is necessary to install the leads 28a, 28b, 28c, and 28d in the manufacturing processes of a package, the manufacturing processes are complicated, and it is difficult to match the impedance with an external circuit. In consideration of the above-mentioned problems, the purpose of the present invention is to provide a package structure that can be surface-mounted and has an easy impedance matching.

[0007]

(Means to solve the problems)

In order to achieve the above-mentioned purpose, the package structure of the present invention is equipped with each element of (a) a semiconductor chip, (b) an insulating substrate in which said semiconductor chip is placed on the surface and which has first through holes for a signal line and second through holes for a ground, (c) a back face-side ground pattern formed on the back face of the above-mentioned insulating substrate, (d) a surface-side ground pattern which is formed in a region including the peripheral edge part of the surface of the above-mentioned insulating substrate and connected to the above-mentioned back face-side ground pattern via a conductor in the above-mentioned second through holes, (e) a surface-side signal line which is formed on the surface of the above-mentioned insulating substrate, connected to an input terminal or output terminal of the above-mentioned semiconductor chip, and forms a transmission line with the above-mentioned surface-side ground pattern and/or the above-mentioned back face-side ground pattern, (f) a back face-side signal line which is formed on the back face of the above-mentioned insulating substrate, connected to the above-mentioned surface-side signal line via a conductor in the above-mentioned first through holes, and forms a microstrip line with the above-mentioned surface-side ground pattern, and (g) an electroconductive cap which covers the above-mentioned semiconductor chip on the above-mentioned insulating substrate and the above-mentioned surface-side signal

line and is connected to the above-mentioned surface-side ground pattern.

[0008]

(Operation)

In the package structure of the present invention, the surface-side signal line forms a transmission line such as microstrip line and coplanar strip line with the surface-side ground pattern and/or the back face-side ground pattern, and the back face-side signal line forms a microstrip line with the surface-side ground pattern. Furthermore, since the surface-side signal line and the back face-side signal line are connected via the conductor in the through holes, the characteristic impedance is adjusted by the size of the through holes, etc., so that the impedance can be easily matched with an external circuit. Also, the package structure is placed on the circuit substrate, and the back face-side signal line and the wiring pattern on the circuit substrate are connected by soldering, etc., so that the surface mounting is realized.

[0009]

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(Application example)

Next, referring to the attached figures showing an application example of the present invention, the application example of the present invention is explained. Figure 1 is an oblique view showing a package structure 40 of an application example of the present invention. Figure 2 is a cross section of II-II of Figure 1.

[0010] The package structure 40 is equipped with an insulating substrate 44 on which a semiconductor chip 42 is placed, a surface-side signal line 46 formed on the insulating substrate 44, a surface-side ground pattern 48 formed on the surface of the insulating substrate 44 so that the surface-side signal line 46 may be enclosed, a back face-side signal line 50 (see Figure 2) which is formed on the back face of the insulating substrate 44 and connected to the surface-side signal line 46, a back face-side ground pattern 52 (see Figure 2) which is formed on the back face of the insulating substrate 44 and connected to the surface-side ground pattern 48, and an electroconductive cap 54 which covers the semiconductor chip 42 on the insulating substrate 44 and the surface-side signal line 46 and is connected to the surface-side ground pattern 48.

[0011] The insulating substrate 44 has several first through holes 56 (see Figure 2) for a signal line and several second through holes 58 (see Figure 1) for a ground. Also, the surface-side signal line 46 is connected to the input terminal or output terminal of the semiconductor chip 42, and the surface-side signal line 46 forms a microstrip line with the back face-side ground pattern 52. Also, the back face-side signal line 50 is connected to the surface-side signal line 46 via a conductor in the first through holes 56 and forms a microstrip line with the surface-side ground pattern 48. Since the microstrip line, as shown in Figures 1 and 2, is formed on a protruded part 60, the position during the surface mounting is easily detected, so that

the yield can be improved. Also, the back face-side ground pattern 52 is connected to the surface-side ground pattern 48 via a conductor in the second through holes 58.

[0012] Next, the method for manufacturing the package structure 40 of this application example is explained. First, the external shape of the insulating substrate 44 such as alumina substrate and the through holes 56 and 58 are worked by a CO₂ gas laser. Next, the surface-side signal line 46 is metalized by a thick film conductor of Au, and the surface-side ground pattern 48, back face-side signal line 50, back face-side ground pattern 52, and through holes are formed by an Ag-Pd thick film conductor. Next, the semiconductor chip 42 such as monolithic microwave integrated circuit is die-bonded on the insulating substrate 44 by an eutectic solder such as Au-Sn and bonding-wired by an Au wire of 25 $\mu\text{m}\phi$. Then, the electroconductive cap 54 is welded onto the surface-side ground pattern 48 by a parallel seam welding method, so that a package structure is completed. Then, the back face side of the insulating substrate 44 is soldered to a mother board on which a pattern matched with the back face pattern of the insulating substrate 44 is formed by an eutectic solder such as Sn-Pb.

[0013] Also, the shape of the protruded part 60 of the package structure 40 of this application example may be the shape of a protruded part as shown in Figure 3. A modified example of the insulating substrate 44 is shown in Figure 4. As seen from Figure 4, a substrate can also be formed by superposing two

sheets of insulating substrates 64 and 66. In this case, through holes are formed in each insulating substrate 64 and 66, and signal lines of the surface and the back face are connected.

[0014] Next, an example in which ceramic is used as the material of the cap is shown in Figure 5. In a cap 70 made of the ceramic, its inner wall 72 or outer wall 74 is metalized (the outer wall is metalized in Figure 5), and the surface metalized is connected to the ground pattern of the surface of the insulating substrate 44, so that an electromagnetic blocking effect can be obtained. The cap 70 is metalized by plating, spreading of an electroconductive paint, spreading a thick film paste, etc.

[0015] Also, in the package structure of the above-mentioned application example, a microstrip line is formed between the surface-side signal line 46 and the back face-side ground pattern 52, however a coplanar strip line between the surface-side signal line and the surface-side ground pattern and a grounded coplanar strip line between the surface-side signal line and the surface-side and back face-side ground pattern may also be formed.

[0016] Also, the surface-side signal line and the back face-side signal line are connected via the conductor in the through holes, the characteristic impedance can be matched with 50Ω , for instance, by adjusting the size of the through holes, etc. Also, since the surface-side ground pattern and the back face-side ground pattern are connected via the conductor in the through holes, the ground of the surface can be reinforced by increasing

the number of said through holes.

[0017]

(Effects of the invention)

As explained above, according to the package structure of the present invention, a transmission line such as microstrip line is formed over the surface-side signal line and the back face-side signal line, and the characteristic impedance can be adjusted by the through holes. Therefore, with the adjustment of the impedance of an external circuit to a prescribed impedance, the impedance with the external circuit is easily matched.

[0018] Also, the package structure is placed on the circuit substrate, and the back face-side signal line and the wiring pattern on the circuit substrate can be connected by solder, etc., so that the surface mounting can be made easy.

4. Brief description of the figures

Figure 1 is an oblique view showing the package structure.

Figure 2 is a cross section of II-II of Figure 1.

Figure 3 is an oblique view showing a modified example of a protruded part.

Figure 4 is a cross section showing the case where two sheets of insulating substrate are superposed.

Figure 5 is a cross section showing the case where a ceramic cap is used.

Figure 6 shows a conventional package structure before being covered with a cap.

Figure 7 is a cross section showing the case where the cap is covered on the substrate shown in Figure 6.

Figure 8 is an oblique view showing another conventional package structure.

Explanation of numerals:

- 40 Package structure
- 42 Semiconductor chip
- 44 Insulating substrate
- 46 Surface-side signal line
- 48 Surface-side ground pattern
- 50 Back face-side signal line
- 52 Back face-side ground pattern
- 54 Electroconductive cap
- 56, 58 Through holes

*** ERROR TX REPORT ***

TX FUNCTION WAS NOT COMPLETED

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|----------------|-------------|--------------|
| TX/RX NO | 1518 | |
| CONNECTION TEL | | 912022837860 |
| SUBADDRESS | | |
| CONNECTION ID | | |
| ST. TIME | 02/10 12:50 | |
| USAGE T | 00'00 | |
| PGS. | 0 | |
| RESULT | NG | |
| | 0 | #018 |

1 OF 13

To:
Attorney Mr. John Dresch (Reg. Nr.: 46,672)
SUGHRUE MION, PLLC
Fax Nr.: 202-283-7860

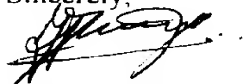
Topic: 09/664,094 (Docket No.: Q60884) / Certified Translation of Japanese Document
No. 5-166965

Date: February 10, 2003

Dear Mr. Dresch:

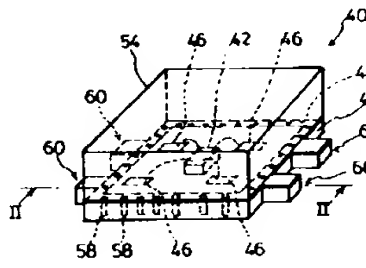
With reference to our recent interview and interview summary on application 09/664,094,
please find the title page and 11 pages comprising the entire certified translation of
Japanese Doc. 5-166965.

Sincerely,

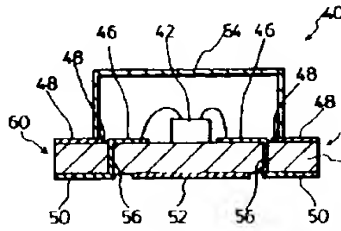


Johannes P. Mondt, Patent Examiner for 09/664,094 (Docket No.: Q60884) at Art Unit
2826.
(Tel. No.: (703-)306-0531)

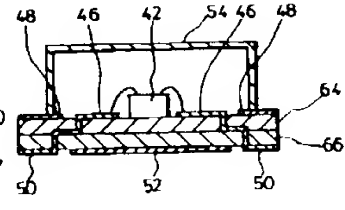
【図1】



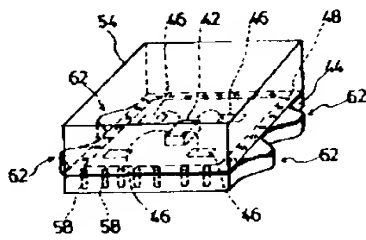
【図2】



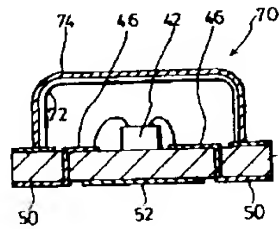
【図4】



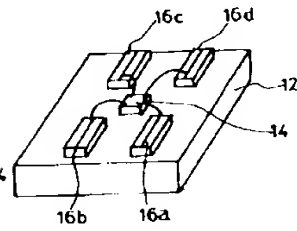
【図3】



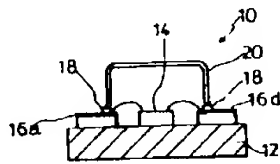
【図5】



【図6】



【図7】



【図8】

